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DATA DRIVER OF MATRIX TYPE DISPLAY DEVICE

[Matorikusu Gata Hyoshi Sochi No Deta Doraiba]

Kazuhiro Takahara and Tadahisa Yamaguchi

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/1[1]

Specification

1. Title of the invention

DATA DRIVER OF MATRIX TYPE DISPLAY DEVICE

2. Claim

A data driver of a matrix type display device, characterized by the fact that in a data driver of a matrix type display device that applies a data voltage to a data bus (1) of a matrix type display panel (3) in which the above-mentioned data bus (1) and a scan bus (2) are orthogonally arranged, it is equipped with a sample-and-hold circuit (4) that samples a display data in accordance with the above-mentioned data bus (1) and applies a data voltage to said data bus (1); several shift registers (5-1 to 5-n) that apply sampling pulses to said sample-and-hold circuit (4); and a selecting circuit (6) that applies shift clock signals with each same phase to said several shift registers (5-1 to 5-n) and sets them to a simultaneous sampling mode or applies shift clock signal with each different phase and sets them to a sequential sampling mode.

[1] Numbers in the margin indicate pagination in the foreign text.

3. Detailed explanation of the invention

(Outline)

The present invention pertains to a data driver of a matrix type display device for applying a data voltage to a data bus of a display panel.

Its purpose is to provide an economical data driver that can switch a simultaneous sampling mode and a sequential sampling mode.

Its constitution is characterized by the fact that in a data driver of a matrix type display device that applies a data voltage to a data bus of a matrix type display panel in which the above-mentioned data bus and a scan bus are orthogonally arranged, it is equipped with a sample-and-hold circuit that samples a display data in accordance with the above-mentioned data bus and applies a data voltage to said data bus; several shift registers that apply sampling pulses to said sample-and-hold circuit; and a selecting circuit that applies shift clock signals with each same phase to said several shift registers and sets them to a simultaneous sampling mode or applies shift clock signal with each different phase and sets them to a sequential/2 sampling mode.

(Industrial application field)

The present invention pertains to a data driver of a matrix type display device for applying a data voltage to a data bus of a display panel.

In the matrix type display panel, a data bus and a scan bus are orthogonally arranged, and as a display medium, a liquid crystal display panel in which a liquid crystal is interposed at the intersection of the data bus and the scan bus is general. Also, there are an active matrix type in which switching elements such as thin film transistors are installed at the intersection of the data bus and the scan bus and a simple matrix in which such a switching element is not installed. Also, a constitution in which a full-color display is made possible by installing a color filter.

Since the matrix type display panel is a thin type, it is applied to display devices such as small-scale color television receivers and personal computers. Also, the development as a full-color video projector is advanced.

Therefore, it is desirable for a data driver for driving the matrix type display panel to be able to be applied to various kinds of usages.

(Prior art)

A dada driver of a matrix type display device of a conventional example, for example, as shown in Figure 8,

consists of a sample-and-hold circuit 54 and a shift register 55, and the sample-and-hold circuit 54 consists of sampling switch 56, sampling capacitor 57, and buffer amplifier 58. Also, in a matrix type display panel 53, a display medium such as liquid crystal is interposed at the intersection of a data bus 51 and a scan bus 52, and a scan voltage is sequentially applied to the scan bus 52 from the scan driver 59.

Also, as a display data, the case where signals of R (red), G (green), and B (blue) are input is shown, and a shift data S1 is added to the shift register 55 by synchronizing with a synchronous signal of the display data, sequentially shifted by a shift clock signal CLK, and output as a sampling pulse from each stage of the shift register 55. A sampling switch 56 is turned on by the sampling pulse, and the display data is added to the sampling capacitor 57 and sampled and held. The voltage sampled and held is applied as a data voltage to the data bus 51 via a buffer amplifier 58.

Images and characters are displayed by the combination of display cells of the intersection of the data bus 51 to which the data voltage is applied and the scan bus 52 to which the scan voltage is applied.

Figure 9 is an illustrative diagram showing a sampling operation. Analog R, G, and B signals separated from a

composite picture signal such as color video signal are sequentially sampled, and a shift data S1 of "1" is sequentially shifted by a shift clock signal CLK, and output signals S1, S2, S3, etc., of each stage of the shift register 55 become "1," so that the level of a round mark of the R, G, and B signals is sampled and held.

Figure 10 shows the case where a composite picture signal is separated into a synchronous signal SYN and luminance signals of R, G, and B, and the R, G, and B signals are shown at the same level or levels corresponding to the luminance. Also, in case the R, G, and B signals at the same level are simultaneously obtained, that is, in case R + G + B is shown, a white display is attained. In case these R, G, and B signals are sequentially sampled, a correct sample hold output signal cannot be obtained by the transmission distortion of a waveform.

For example, as shown in Figure 11, in case signals shown by RGB are sampled at time t1, t2, and t3 from output signals S1, S2, and S3 of the shift register 55, sample hold output signal at each prescribed level can be obtained. However, if a waveform rounding is generated like a waveform shown by RGB' by electrostatic capacitance of a transmission line, etc., the sample hold output signal at time t1 has a low level, compared with the RGB signal in which no waveform rounding is generated.

For example, in case R signal is sampled and held at time t1, G signal is sampled and held at time t2, and B signal is sampled/3 and held at time t3, the level of the sample hold output signal of R signal is lowered, so that a correct color display is impossible.

Accordingly, a constitution in which R, G, and B signals are simultaneously sampled has been used. In other words, for a signal in which the wave rounding is generated like RGB' signal, R, G, and B signals are simultaneously sampled and held at a time of a prescribed level like time t2.

(Problems to be solved by the invention)

The data driver of the matrix type display device of the conventional example has a constitution of one of the sequential sampling and the simultaneous sampling. In the data driver of the sequential sampling method, as mentioned above, it is difficult to obtain a precise sample hold output signal by the waveform rounding, and in the data driver of the simultaneous sampling method, since the sampling interval is lengthened, the resolution is lowered in a two-color display such as white and black.

Also, the number of data bus 51 is increased with the increase of the display capacity of the matrix type display panel 53, and it is necessary to rise the frequency of the shift

clock CLK of the shift register 55. However, since there was a limitation in raising the frequency, a limitation was also caused in the display capacity of the matrix type display panel that could be driven by the data driver.

The purpose of the present invention is to provide an economical data driver that can switch a simultaneous sampling mode and a sequential sampling mode.

(Means to solve the problems)

In the data driver of the matrix type display device of the present invention, several shift registers are installed, and the present invention is explained referring to Figure 1.

In the data driver of the matrix type display device that applies a data voltage to a data bus 1 of a matrix type display panel 3 in which the data bus 1 and a scan bus 2 are orthogonally arranged, it is equipped with a sample-and-hold circuit 4 that samples a display data in accordance with the data bus 1 and applies a data voltage to said data bus 1, several shift registers 5-1 to 5-n that apply sampling pulses to said sample-and-hold circuit 4, and a selecting circuit 6 that applies shift clock signals with each same phase to said several shift registers 5-1 to 5-n and sets them to a simultaneous sampling mode or applies shift clock signal with each different phase and sets them to a sequential sampling mode. 7 is a scan

driver that sequentially selects the scan bus 2 and applies a scan voltage.

(Operation)

Shift clock signals with the same phase or each different phase are selected and added to several shift registers 5-1 to 5-n by the selecting circuit 6, and output signals at each stage of several shift registers 5-1 to 5-n are added as sampling pulses to the sample-and-hold circuit 4, and a display data is sampled and added as a data voltage to the data bus 1 of the matrix type display panel 3.

Since each shift register 5-1 to 5-n may be operated by a shift clock signal with a frequency of 1/n, compared with a conventional example using one shift register, the data driver for the matrix type display panel 3 with a large display capacity can be easily constituted.

Also, in case shift clock signals with the same phase are added to several shift registers 5-1 to 5-n, since the output signals of each stage of several shift registers 5-1 to 5-n have the same phase, the display data can be simultaneously sampled in the sample-and-hold circuit 4. In other words, if the shift clock signals with each different phase are added to several shift registers 5-1 to 5-n, since the output signals of each stage of several shift registers 5-1 to 5-n are different

phases, the display data can be sequentially sampled in the sample-and-hold circuit 4. In other words, a sequential /4 sampling mode is set. Therefore, a shift clock signal is selected by the selecting circuit 6 and added to several shift registers 5-1 to 5-n, so that the display data is sampled at one of the simultaneous sampling mode and the sequential sampling mode, thereby being able to apply a data voltage to the data bus 1.

(Application example)

Next, application examples of the present invention are explained in detail, referring to the figures.

Figure 2 is a block diagram showing the main parts of an application example of the present invention. 11 is a data bus, 12 is a scan bus, 13 is a matrix type display panel, 14 is a sample-and-hold circuit, 15-1 to 15-3 are shift registers, 16 is a selecting circuit for selecting shift block signals CLK1-CLK3, 17 is a scan driver, SW1-SWm are sampling switches consisting of transistors, C1-Cm are sampling capacitors, and BF1-BFm are buffer amplifiers.

This application example shows the case where the shift registers 15-1 to 15-3 are installed in accordance with R, G, and B signals, and each shift register 15-1 to 15-3 has a constitution of m/3 stages. Also, the matrix type display panel

13, for example, can be an active matrix type liquid crystal display panel which consists of m pieces of data buses 11 and k pieces of scan buses 12 and in which display cells of m x k are constituted and color filters of R, G, and B are installed.

The scan driver 17 has a constitution in which k pieces of scan buses 12 are sequentially selected by synchronizing with a synchronous signal of a display data and applying a scan voltage, and a data voltage corresponding to the display data is simultaneously applied to m pieces of data bus 11 from the sample-and-hold circuit 14 by synchronizing with the scan voltage. The sample-and-hold circuit 14 consists of the sampling switches SW1-SW2 consisting of transistors being driven by output signals of the shift registers 15-1 to 15-n, the sampling capacitors C1-Cm for sampling and holding, and the buffer amplifiers BF1-BFm for outputting a data voltage.

Also, the shift registers 15-1 to 15-3 shift the shift data 1 synchronized with the synchronous signal of the display data according to the shift clock signal and adds the output signals of each stage as sampling pulses to the sampling switches SW1-SWm of the sample-and-hold circuit 14. For example, the output signal of the first stage of the shift register 15-1 is added to the sampling switch SW1, the output signal of the second stage is added to the sampling switch SW4, the output signal of the

third stage is added to the sampling switch SW7 (not shown in the figure), ..., and the output signal of the m/3rd stage of the final stage is added to the sampling switch SWm-2. Also, the output signal of the first stage of the shift register 15-2 is added to the sampling switch SW2, the output signal of the second stage is added to the sampling switch SW5 (not shown in the figure), ..., and the output signal of the m/3rd stage of the final stage is added to the sampling switch SWm-1. Also, the output signal of the first stage of the shift register 15-3 is added to the sampling switch SW3, ..., and the output signal of the m/3rd stage of the final stage is added to the sampling switch SWm.

Also, the shift clock signals CLK1-CLK3 with each different phase are input into the selecting circuit 16, and if one of them, for example, the shift clock signal CLK1 is selected and added to each shift register 15-1 to 15-3, the output signals of each stage corresponding to each shift register 15-1 to 15-3 have the same phase. For example, the output signals of one stage of each shift register 15-1 to 15-3 are added to the sampling switches SW1, SW2, and SW3 and simultaneously turned on, and R, G, and B signals are simultaneously sampled and held by the sampling capacitors C1, C2, and C3. If the next shift clock signal CLK1 is added, the output signals of the second

stage of each shift register 15-1 to 15-3 are added to the sampling switches SW4, SW5, and SW6 (not shown in the figure) and simultaneously turned on. Therefore, a simultaneous sampling mode is set. /5

Also, if the shift clock signals CLK1-CLK3 are respectively added to the shift registers 15-1 to 15-3 by the selecting circuit 16, the output signals of each stage corresponding to each shift register 15-1 to 15-3 have different phases. For example, if the initial shift clock signal CLK1-CLK3 are sequentially added to the shift registers 15-1 to 15-3, the output signals of the first stage of the shift registers 15-1 to 15-3 are sequentially added to the sampling switches SW1-SW3, R signal is sampled by the sampling switch SW1, G signal is sampled by the sampling switch SW2, and B signal is sampled by the sampling switch SW3, so that the signals are sequentially sampled at each different phase. In other words, a sequential sampling mode is set.

Figure 3 is an illustrative diagram showing the simultaneous sampling mode. (a) is a display data, (b) is a shift data S1, (c)-(e) are shift clock signals being added to the shift registers 15-1 to 15-3, and (f)-(h) are sample hold output signals. The shift clock signals with the same phase shown in (c)-(e) are added to each shift register 15-1 to 15-3,

the shift data shown in (b) is sequentially shifted, a simultaneous sampling of R, G, and B is carried out by the output signals of each stage of each shift register 15-1 to 15-3, so that the sample hold output signals shown in (f)-(g) are obtained.

Figure 4 is an illustrative diagram showing the sequential sampling mode. (a) is a display data, (b) is a shift data S1, (c)-(e) are shift clock signals being added to the shift registers 15-1 to 15-3, and (f)-(h) are sample hold output signals. Since the shift clock signals with different phases shown in (c)-(e) are added to each shift register 15-1 to 15-3, the output signals of each stage of the shift registers 15-1 to 15-3 also have different phases and are sampled in the sequence of R, G, B, R, G, B, ···. In other words, a sequential sampling mode is set.

Therefore, with the selection of a shift clock signal by the selecting circuit 16, any of the simultaneous sampling mode and the sequential sampling mode can be operated. Also, since the shift clock signal is good at a frequency of 1/3, compared with the conventional example, if the shift register with the same operation speed as that of the conventional example is used, a matrix type display panel in which the number of data bus 11 is three times can also be easily driven.

Figure 5 is a clock diagram showing the main parts of another application example of the present invention. 21 is a data bus, 22 is a scan bus, 23 is a matrix type display panel, 24 and 34 are sample-and-hold circuits, 25-1 to 25-3 and 31-5 to 35-3 are shift registers, 26 and 36 are selecting circuits, and 27 is a scan drier.

If the data bus 21 is set to 21-1 to 21-m from the left, odd data buses 21-1, 21-3, etc., are connected to the sample-and-hold circuit 24, and even data buses 21-2, 21-4, etc., are connected to the sample-and-hold circuit 34.

Also, shift clock signals CLK1-CLK3 and CLK1'-CLK3' being input into the selecting circuits 26 and 36 have each different phase, and at the simultaneous sampling mode, the shift clock signals are selected by the selecting circuits 26 and 36 so that the shift clock signals being added to the shift registers 25-1, 25-3,and 35-2 may have the same phase and the shift clock signals being added to the shift registers 25-2, 35-1,and 35-3 may have the same phase. In this case, in the display data input into the sample-and-hold circuits 24 and 34, R, G, and B signals are simultaneously sampled in accordance with the data buses 21-1, 21-2, and 21-3, and R, G, and B signals are simultaneously sampled in accordance with the data buses 21-4, 21-5, and 21-6. Also, at the sequential sampling mode, the

shift clock signals are selected by the selecting circuits 26 and 36 so that all the shift clock signals being added to the shift registers 25-1 to 25-3 and 35-1 to 35-3.

Figure 6 is an illustrative diagram showing the simultaneous sampling mode. (a) is a display data, (b) is a shift data S1, (c)-(e) are shift clock signals being added to /6 the shift registers 25-1 to 25-3 from the selecting circuit 26, (f)-(h) are sample hold output signals of the sample-and-hold circuit 24, (l)-(k) are shift clock signals being added to the shift registers 35-1 to 35-3 from the selecting circuit 36, and (l)-(n) are sample hold output signals of the sample-and-hold circuit 34.

For the display data RG1 shown in (a), since the shift data S1 is shifted by the shift clock signals shown in (c), (e), and (j) and sampled by the output signals of the first stage of the shift registers 25-1, 25-3, and 35-2, sample hold output signals shown by R1, B1, and G1 of (f), (h), and (m) are attained. Since the shift data S1 is shifted by the shift clock signals (d), (i), and (k) and sampled by the output signals of the first stage of the shift registers 25-2, 35-1, and 35-3, sample hold signals shown by G2, R2, and B2 of (g), (l), and (n) are attained.

Figure 7 is an illustrative diagram showing the sequential sampling mode. (a) is a display data, (b) is a shift data S1, (c)-(e) are shift clock signals being added to the shift registers 25-1 to 25-3 from the selecting circuit 24, (f)-(h) are sample hold output signals of the sample-and-hold circuit 24, (l)-(k) are shift clock signals being added to the shift registers 35-1 to 35-3 from the selecting circuit 36, and (l)-(n) are sample hold output signals of the sample-and-hold circuit 34.

As shown in (c)-(e) and (i)-(k), the shift clock signals being added to the shift registers 25-1 to 25-3 and 35-1 to 35-3 have each different phase, and display data R_1, G_1, and B_1 shown in (a) are sequentially sampled by the output signals of the first stage of the shift registers 25-1, 25-3, and 35-2, so that sample hold output signals shown in (f), (l), and (g) are attained. Also, display data R_2, G_2, and B_2 shown in (a) are sequentially sampled by the output signals of the first stage of the shift registers 25-2, 35-1, and 35-3, so that sample hold output signals shown in (m), (h), and (n) are attained.

Therefore, with the selection of shift clock signals by the selecting circuits 26 and 36, any of the simultaneous sampling mode and the sequential sampling mode can be selected.

The present invention is not limited to only the above-mentioned application examples but can be variously added and changed. For example, the frequency of shift clock signals can be further reduced to half by further doubling the number of shift register. Also, since the shift registers do not shift a display data but only shift the shift data S1 of one bit, the constitution is relatively simple.

(Effects of the invention)

As explained above, several shift registers 5-1 to 5-n are installed, and when shift clock signals with the same phase are added to each shift register 5-1 to 5-n, since the output signals of each stage of each shift register 5-1 to 5-n have the same phase, a simultaneous sampling mode is set. Also, when respective different shift clock signals are added to each shift register 5-1 to 5-n, since the output signals of each stage of each shift register 5-1 to 5-n have each different phase, a sequential sampling mode is set. This mode can be switched by selecting the above-mentioned shift clock signals by the selecting circuit 6.

Therefore, if the frequency of the shift clock signals is the same as that of the conventional example, since the matrix type display panel 3 having the data buses 1 of twice of the number of shift registers 5-1 to 5-n can be driven, the display

capacitance can be increased. Also, since any of the simultaneous sampling mode and the sequential sampling mode can be operated by the data driver with the same constitution, the cost can be reduced by the mass production.

4. Brief description of the figures

Figure 1 is an illustrative diagram showing the principle of the present invention. Figure 2 is a block diagram showing an application example of the present invention. Figure 3 is an illustrative diagram showing a simultaneous sampling mode. Figure 4 is an illustrative diagram showing a sequential sampling mode. Figure 5 is a block diagram showing the main parts of another application example of the present invention. Figure 6 is an illustrative diagram showing a simultaneous sampling mode. Figure 7 is an illustrative diagram showing a sequential sampling mode. Figure 8 is a block diagram showing the main parts of a conventional example. Figure 9 is an illustrative diagram showing a sampling operation. Figure 10 is an illustrative diagram showing RGB signals. Figure 11 is an illustrative diagram showing a sequential sampling of RGB signals.

1 Data bus

2 Scan bus

3 Matrix type display panel

4 Sample-and-hold circuit

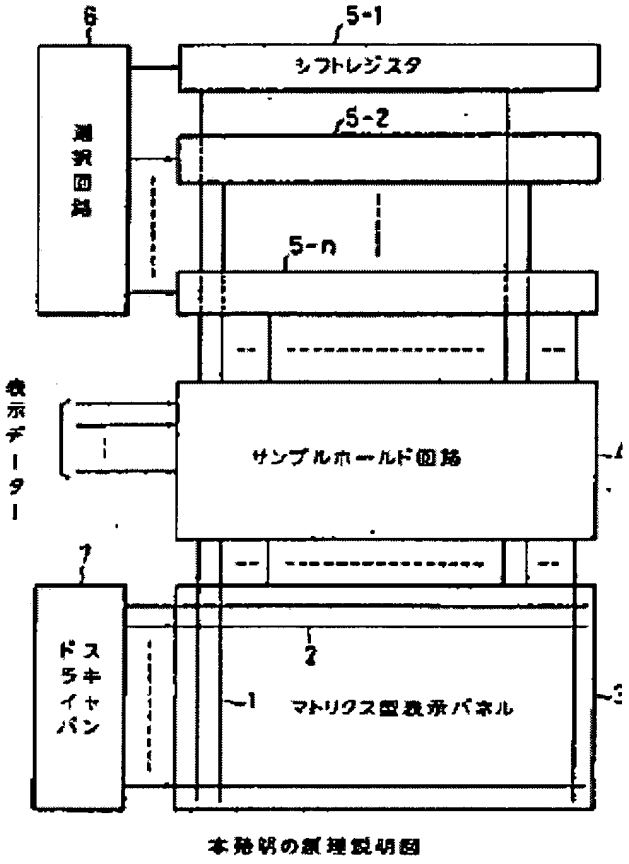
5-1 to 5-n Shift registers

6 Selecting circuit

7 Scan driver

// Insert Figures 1-11 //

Figure 1: An illustrative diagram showing the principle of the present invention



第 1 図

3 Matrix type display panel

4 Sample-and-hold circuit

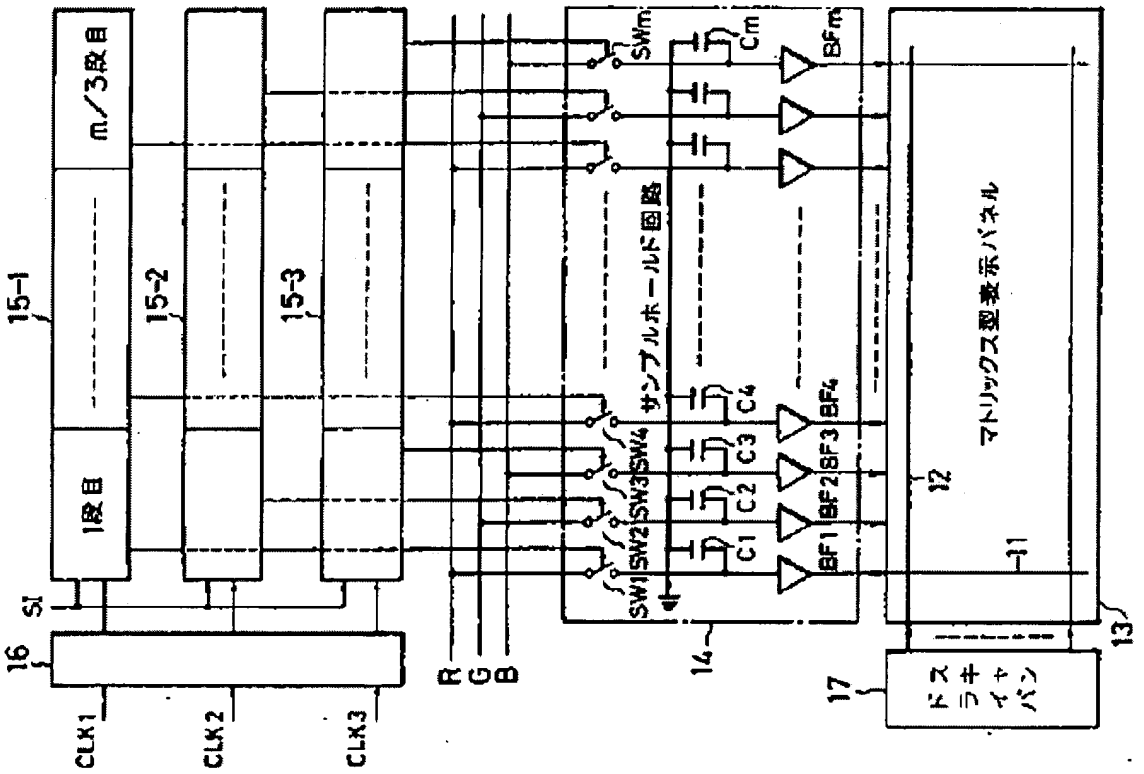
5-1 Shift register

6 Selecting circuit

7 Scan driver

A. Display data

Figure 2: A block diagram showing an application example of the present invention



本発明の一実施例の基部ブロック図

第2図

13 Matrix type display panel

14 Sample-and-hold circuit

17 Scan driver

A. First stage

B. m/3rd stage

Figure 3: An illustrative diagram showing a simultaneous sampling mode

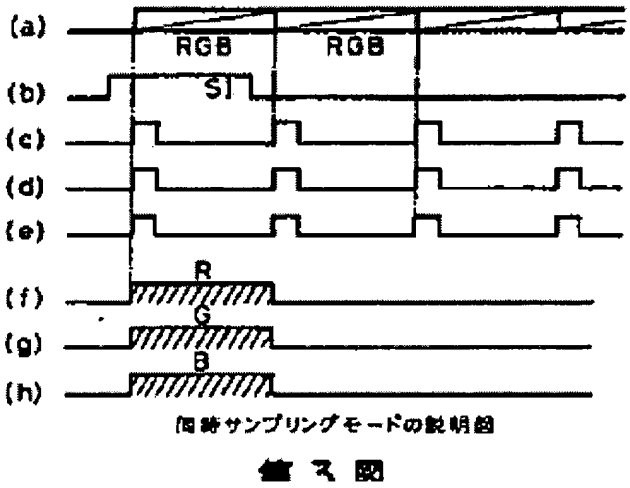


Figure 4: An illustrative diagram showing a sequential sampling mode

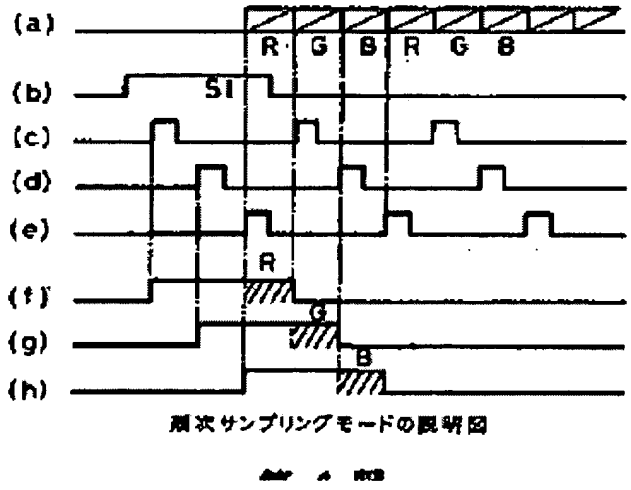
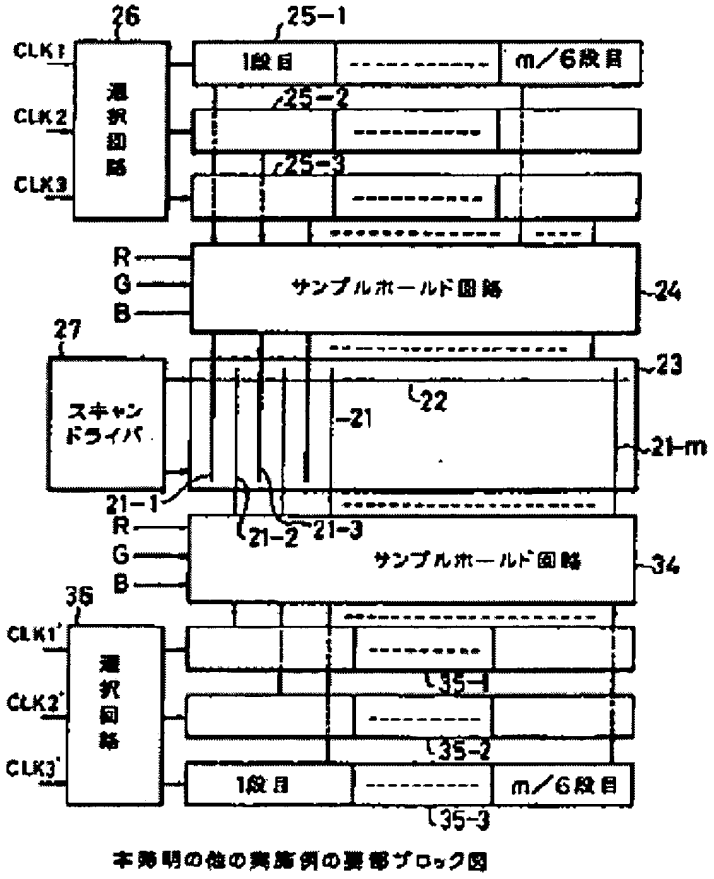


Figure 5: A block diagram showing the main parts of another application example of the present invention



本発明の他の実施例の要部ブロック図

第５図

13 Matrix type display panel

24 Sample-and-hold circuit

26 Selecting circuit

27 Scan driver

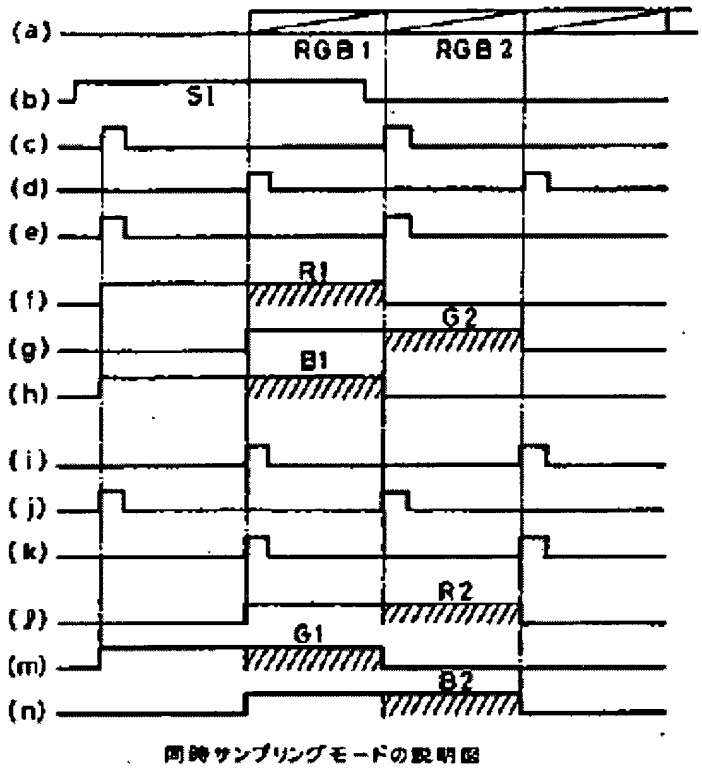
34 Sample-and-hold circuit

36 Selecting circuit

A. First stage

B. m/6th stage

Figure 6: An illustrative diagram showing a simultaneous

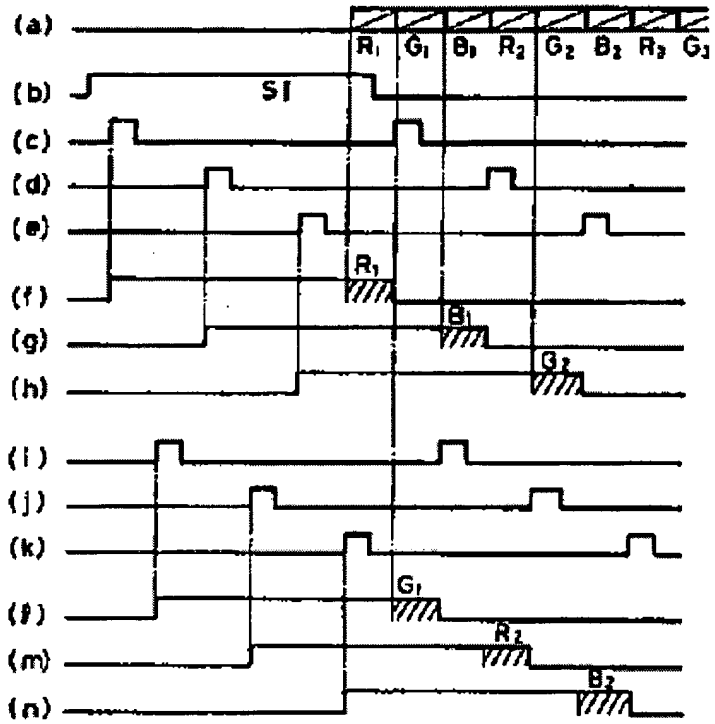


同時サンプリングモードの説明図

第６図

sampling mode

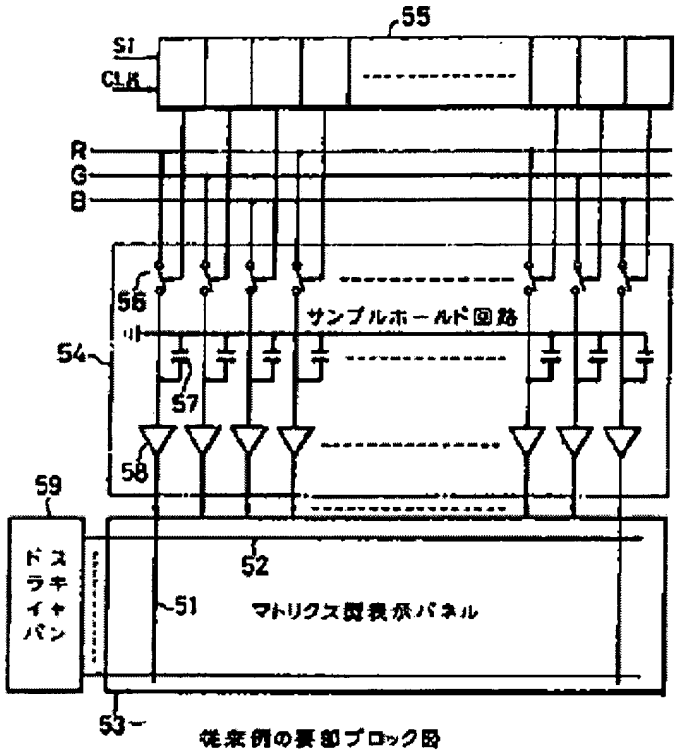
Figure 7: An illustrative diagram showing a sequential sampling mode



順次サンプリングモードの説明図

第 7 図

Figure 8: A block diagram showing the main parts of a conventional example



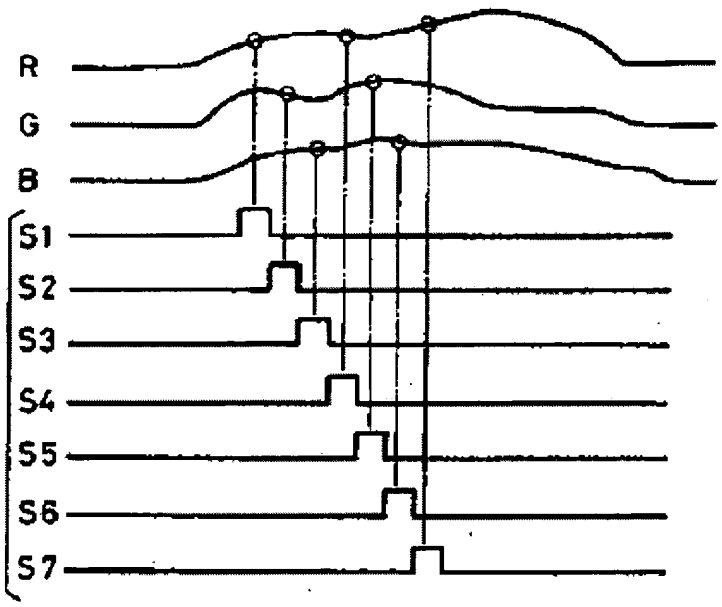
第８図

53 Matrix type display panel

54 Sample-and-hold circuit

59 Scan driver

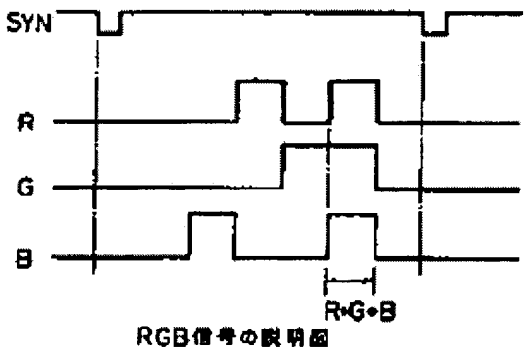
Figure 9: An illustrative diagram showing a sampling operation



サンプリング動作説明図

第 9 図

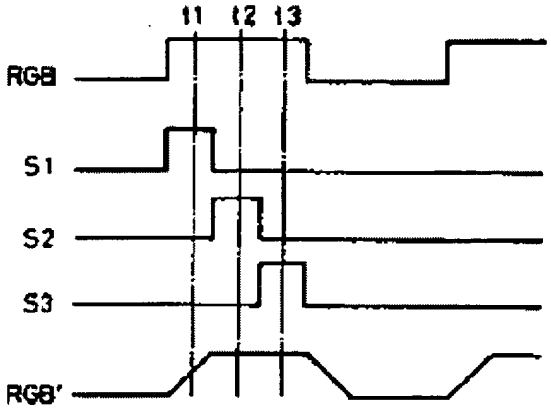
Figure 10: An illustrative diagram showing RGB signals



RGB信号の説明図

第 10 図

Figure 11: An illustrative diagram showing a sequential sampling of RGB signals



RGB信号の順次サンプリングの説明図

第11図